



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/780,057	02/17/2004	Seong-jin Jang	5649-1204	9675
7590	05/09/2005		EXAMINER TAN, VIBOL	
David K. Purks Myers Bigel Sibley & Sajovec Post Office Box 37428 Raleigh, NC 27627			ART UNIT 2819	PAPER NUMBER

DATE MAILED: 05/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H.A

Office Action Summary

Application No.

10/780,057

Applicant(s)

JANG, SEONG-JIN

Examiner

Vibol Tan

Art Unit

2819

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 17 February 2004.
 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-22 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) ☒ Claim(s) 1-9 and 16-22 is/are allowed.
 6) ☒ Claim(s) 10, 11 and 15 is/are rejected.
 7) ☒ Claim(s) 12-14 is/are objected to.
 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) ☒ All b) ☐ Some * c) ☐ None of:
 1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
 * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
 Paper No(s)/Mail Date _____.
 4) ☐ Interview Summary (PTO-413)
 Paper No(s)/Mail Date _____.
 5) ☐ Notice of Informal Patent Application (PTO-152)
 6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 10, 11 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art in Fig. 1 in view of Taylor et al. (U. S. PAT. 6,157,206).

In claim 10, Applicant's admitted prior art of Fig. 1 teaches, a semiconductor device, comprising: an input pin (112) that is configured to receive an input signal from external to the semiconductor device; an on-chip termination circuit that comprises a pull-up termination resistor (RU) and a pull-down termination resistor (RD), wherein the pull-up termination resistor and the pull-down termination resistor are connected in series between a first power supply voltage (VDD) and a second power supply voltage (GND), and wherein the input signal is conducted through a connection node (not marked) between the pull-up termination resistor and the pull-down termination resistor; an input buffer (231) that is configured to generate an internal signal (CS1) based on the input signal (112) from the on-chip terminal circuit and a reference voltage (111); with the exception of teaching a reference voltage generator circuit. However, Taylor et al. teaches in Fig. 4, a reference voltage generator that comprises a first resistor (418) and a second resistor (420), wherein the first and second resistors are connected in

Art Unit: 2819

series between the first power supply voltage (406) and the second power supply voltage (GDN), and wherein the reference voltage is generated at a node (434) between the first and second resistors.

Therefore; it would have been obvious to one ordinary skill in the art at the time of the invention was made to implement the reference voltage generator, as taught by Taylor et al., into the device of the prior art, in order to obtain a reference voltage that is half of the first power supply voltage.

In claim 11, Applicant's admitted prior art of Fig. 1 in view of Taylor et al further teaches the semiconductor device of Claim 10, wherein: the pull-up termination resistor has the same resistance as the first resistor; and the pull-down termination resistor has the same resistance as the second resistor. It is obvious to try to match the resistance values of the pull-up termination resistor to the first resistor and the pull-down termination resistor to the second resistor in order to keep the 112 and 111 voltages exactly the same.

In claim 15, Applicant's admitted prior art of Fig. 1 further teaches the semiconductor device of Claim 10, further comprising a push-pull driver (RU, RD) that is connected to the input pin (112), wherein the push-pull driver comprises a pull-up driver (RU) that is connected between the first power supply voltage (VDD) and the input pin (112), and a pull-down driver (RD) that is connected between the input pin (112) and the second power supply voltage (GND).

Art Unit: 2819

3. Claims 12-14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

4. Claims 1-9 and 16-22 appear to comprise allowable subject matter.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vibol Tan whose telephone number is (571) 272-1811.

The examiner can normally be reached on Monday-Friday (7:00 AM-4:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mike J. Tokar can be reached on (571) 272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



VIBOL TAN
PRIMARY EXAMINER